REMARKS

Applicant concurrently files herewith a Petition and fee for a One-Month Extension of Time.

Claims 1-7, 13-16, and 24-25 are all the claims presently pending in the application. New claims 24-24 have been added to more completely define the present invention. Applicant gratefully acknowledges the Examiner's indication that claims 4-5 and 13-15 are allowed and that claim 6 would be allowable if rewritten in independent form. Claim 6 has been rewritten to overcome this rejection and place the claim into condition for allowance.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claim 1 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Yamazaki, et al. (U.S. Patent No. 6,462,723) (hereinafter "Yamazaki").

Claims 2-3, 7 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki, et al., in view of Sakurai, et al. (JP Patent No. 10-290012) (hereinafter "Sakurai").

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

Applicant's invention, as defined for example by independent claim 1 (and substantially similarly by independent claim 16), is directed to a thin film transistor having a back channel electrode (e.g., used in an active matrix type liquid crystal display panel in a non-limiting embodiment).

A feature of the invention is that a voltage of a front channel positioned on the side of a gate wiring of the thin film transistor may be made equal to a voltage of the back channel positioned on the side of a back channel electrode by short-circuiting the back channel

electrode to a gate electrode through a contact-hole provided in a portion of a semiconductor layer forming the thin film transistor.

Further, a feature of the present invention (e.g., as defined by new dependent claims 24-25) is that the portion of the semiconductor layer forming the thin film transistor contact-hole for short-circuiting the back gate electrode and the gate electrode includes an active layer.

An additional feature of the invention is that the semiconductor layer is patterned to have a width equal to that of source and drain electrodes of a thin film transistor between the source and drain electrodes and a gate insulating film.

With such features, a thin film transistor can be provided which is capable of reducing leakage current of a back channel when it is operated continuously (e.g. see page 3, lines 12-15; page 10, lines 7-27; page 11, lines 1-5; page 12, lines 17-27; and page 13, lines 1-7).

An exemplary configuration of the thin film transistor with a back channel electrode is shown in Figs. 2-3 of the application.

The conventional systems, such as those discussed below and in the Related Art section of the present application, do not have such a structure, and fail to provide for such an operation.

Indeed, such features are clearly not taught or suggested by the cited references.

II. THE PRIOR ART REFERENCES

A. The Yamazaki Reference

The Examiner asserts:

> *[regarding claims 1 and 16] Yamazaki disclose in fig. 3 a thin film transistor including a back channel electrode 701, wherein a voltage of a front channel positioned on a side of a gate wiring of said thin film transistor is made equal to a voltage of said back channel positioned on the side of a back channel electrode by short-circuiting said back channel electrode to a gate electrode 703 through a contact-hole 704 provided in a portion of a semiconductor layer 702 forming said thin film transistor.*

However, Applicant respectfully disagrees and submits that the Examiner's assertions are erroneous.

Firstly, as shown in Figs. 1 and 3, Yamazaki discloses an active matrix semiconductor display, such as an active matrix liquid crystal display with TFTs, having a back gate electrode and a gate electrode such that an arbitrary voltage is applied to the back gate electrode.

However, in fundamental contrast to the present invention, Yamazaki nowhere discloses or suggests the structure for short-circuiting the back gate electrode and a gate electrode. Additionally, nowhere does Yamazaki disclose or suggest a contact-hole provided in a portion of a semiconductor layer forming the TFTs for short-circuiting therebetween.

In Yamazaki, the contact holes 704 shown in FIG. 3 are provided to form an electrical contact between the semiconductor active layer 702 and the wiring electrodes 706 for source and drain electrodes. The disclosure of Yamazaki clearly shows that the back gate electrode 701 and the gate electrode 703 are not short-circuited in FIG. 3.

Additionally, Applicant respectfully draws the Examiner's attention to FIG. 1 or FIG. 16 showing a cross-section of a semiconductor device in which Yamazaki nowhere teaches or suggests providing a contact-hole in a portion of an active layer for short-circuiting the back gate electrode and the gate electrode.

Since the objective of Yamazaki is to control the thresholds of TFTs by applying an arbitrary voltage to the back gate electrode, the gate electrode must be electrically separated from the back gate electrode. To this end, it is clear that Yamazaki teaches away from the present invention. As such, it would not have been obvious to modify Yamazaki, absent hindsight, with regard to the 35 U.S.C. § 103 rejection discussed below.

Furthermore, Yamazaki does not teach or suggest the objects of the present invention such as reducing the number of patterning steps and reducing leakage current of a back channel.

Thus, as discussed above, in Yamazaki there is no teaching or suggestion of the significant features of the present invention including that the back

channel electrode and the gate electrode are short-circuited through a contact-hole provided in a portion of a semiconductor layer, as defined by independent claim 1 (and substantially similarly by independent claim 16).

Hence, turning to the clear language of the claims, there is no teaching or suggestion of "*[a] thin film transistor including:*

a back channel electrode,

wherein a voltage of a front channel positioned on the side of a gate wiring of said thin film transistor is made equal to a voltage of said back channel positioned on the side of a back channel electrode by short-circuiting said back channel electrode to a gate electrode through a contact-hole provided in a portion of semiconductor layer forming said thin film transistor " (emphasis Applicant's).

Thus, for the reasons discussed above, Applicant respectfully submits that the Examiner misunderstands the disclosure of Yamazaki, and thus the rejection under 35 U.S.C. § 102(b) based on Yamazaki is erroneous.

Further, with regard to dependent claims 2,3, and 7, rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Sakurai, these claims when taken in combination with claim 1 define additional novel limitations.

Similarly, regarding independent claim 16, rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Sakurai, Applicant notes for the Examiner that Sakurai discloses (e.g., in Fig. 5) a contact hole 7 in the insulating layer 103. However, there is no teaching or suggestion by Sakurai that the contact-hole should be provided in a portion of a semiconductor layer forming a thin film transistor.

Therefore, these references either alone or in combination are much different from the present invention and fail to teach or suggest the claimed invention.

For the reasons stated above, the claimed invention is fully patentable over the cited references.

III. FORMAL MATTERS AND CONCLUSION

The drawings have been objected to because front channel 182 is not shown in Fig. 10 as described in the specification. In response to the Examiner's objections, Applicant files herewith a replacement drawing sheet for Figure 10 showing the front channel 182.

In view of the foregoing, Applicant submits that claims 1-7, 13-16, and 24-25, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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Sean M. McGinn, Esq.
Registration No. 34,386

McGinn & Gibb, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, VA 22182-3817
(703) 761-4100
Customer No. 21254